Comp E 475

Microprocessors

HW6

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https://github.com/Tpaitchadze/475L

Contents

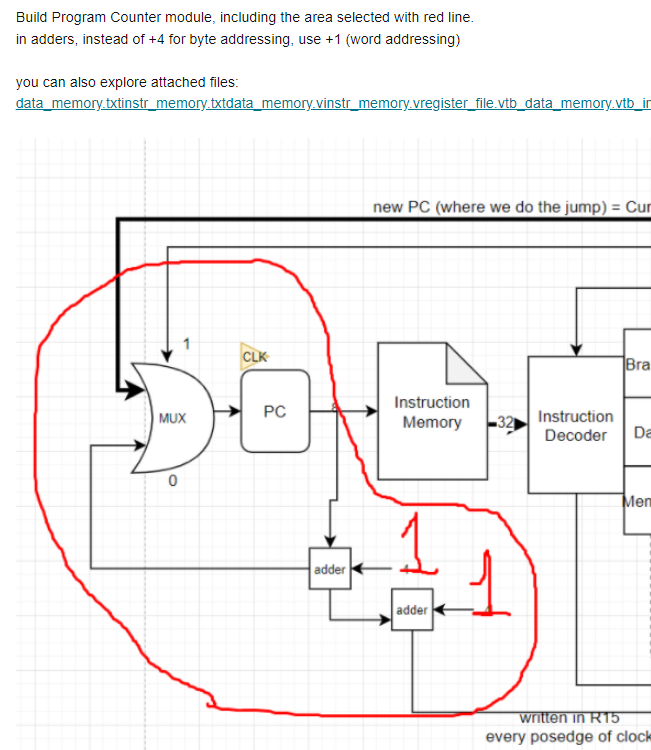
[Task Description 2](#_Toc22460835)

[Solution 2](#_Toc22460836)

[Simulation & Verification 2](#_Toc22460837)

[Comparison 3](#_Toc22460838)

# Task Description



# Solution

To solve the problem I used A B as inputs, as well as clock, Outp and C as outputs. Code itself is very simple and self explanatory.

The code:

`timescale 1ns / 1ps

module HW6(

input A,

input [7:0] B,

input clk,

output reg [7:0] Outp,

output [7:0] C

);

wire [7:0] Temp;

always @ (posedge clk) begin

Outp <= Temp;

end

assign Temp = A ? B : Outp+1;

assign C = Outp+2;

endmodule

# Simulation & Verification

TestBench:

module Test;

reg clk;

reg A;

reg [7:0] B;

wire [7:0] Outp;

wire [7:0] C;

HW6 uut (

.clk(clk),

.A(A),

.B(B),

.C (C),

.Outp (Outp)

);

always #10 clk <= !clk;

always #100 A <= !A;

always #100 B <= B+10;

initial begin

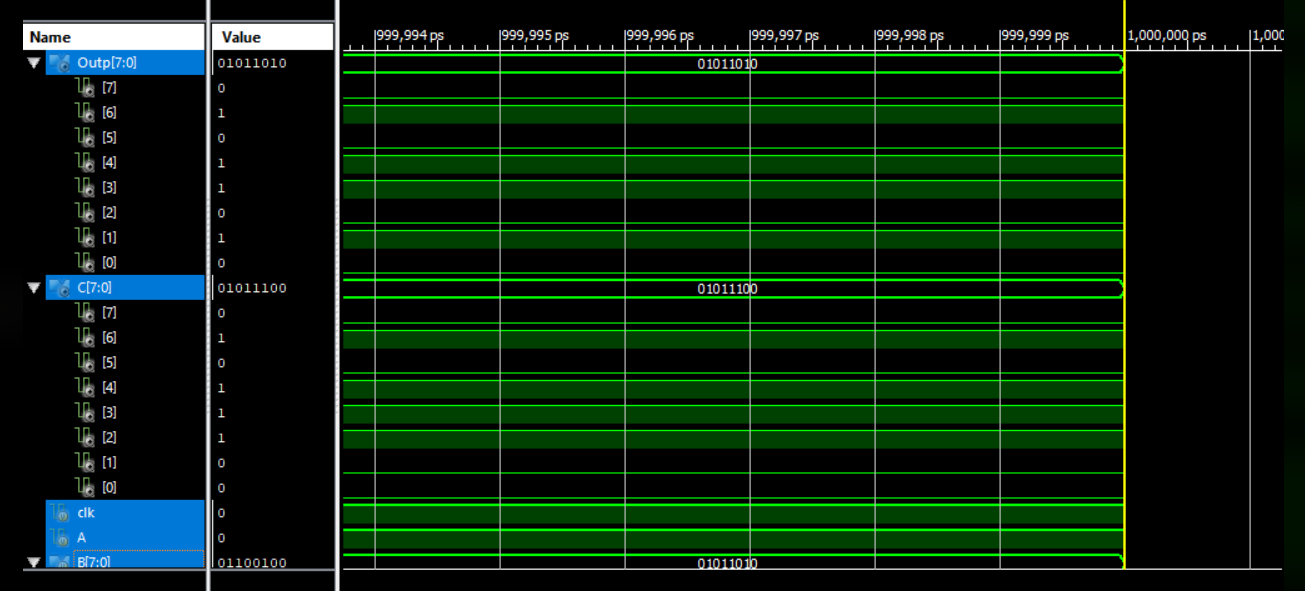
A = 0;

B = 0;

clk = 0;

end

endmodule



# Conclusion

Pc module was surprisingly simple task than other assignments.